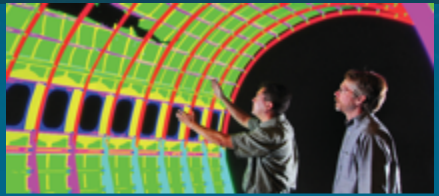
Advanced Microsystems Radiation Effects R&D at Sandia National Laboratories



PRESENTED BY

Nathan Nowlin

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Sandia National Laboratories Leads in National Security Solutions Across the Decades and Across Many Mission Areas

1950s	1960s	1970s	1980s	1990s	2000s	2010s
Nuclear weapons	Development engineering	Multiprogram laboratory	Missile defense work	Post–Cold War transition	START Post 9/11	LEPs Cyber, biosecurity proliferation
Production and manufacturing engineering	Vietnam conflict	Energy crisis	Cold War	Stockpile stewardship	National security	Evolving national security challenges

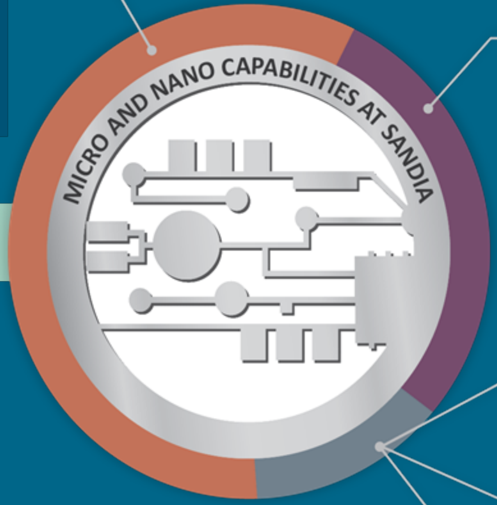
- Sandia National Laboratories is a Department of Energy (DOE) laboratory for weapons, energy, non-proliferation, cyber security, anti-terrorism and many other national security missions
- Initially Z-division of Manhattan Project (Non-nuclear Components)

Our Leadership Stems from a Broad Array of Capabilities and Resources Across Many Disciplines

MESA

MICROSYSTEMS ENGINEERING, SCIENCE, AND APPLICATIONS

- Largest government-owned trusted fabrication facility
- *Supports the most demanding National Security Missions*
- Federally Funded Research & Development Center (FFRDC) with the broadest and deepest micro and nano expertise



CDC

COUNTERFEIT DETECTION CENTER

CINT

CENTER FOR INTEGRATED NANOTECHNOLOGIES

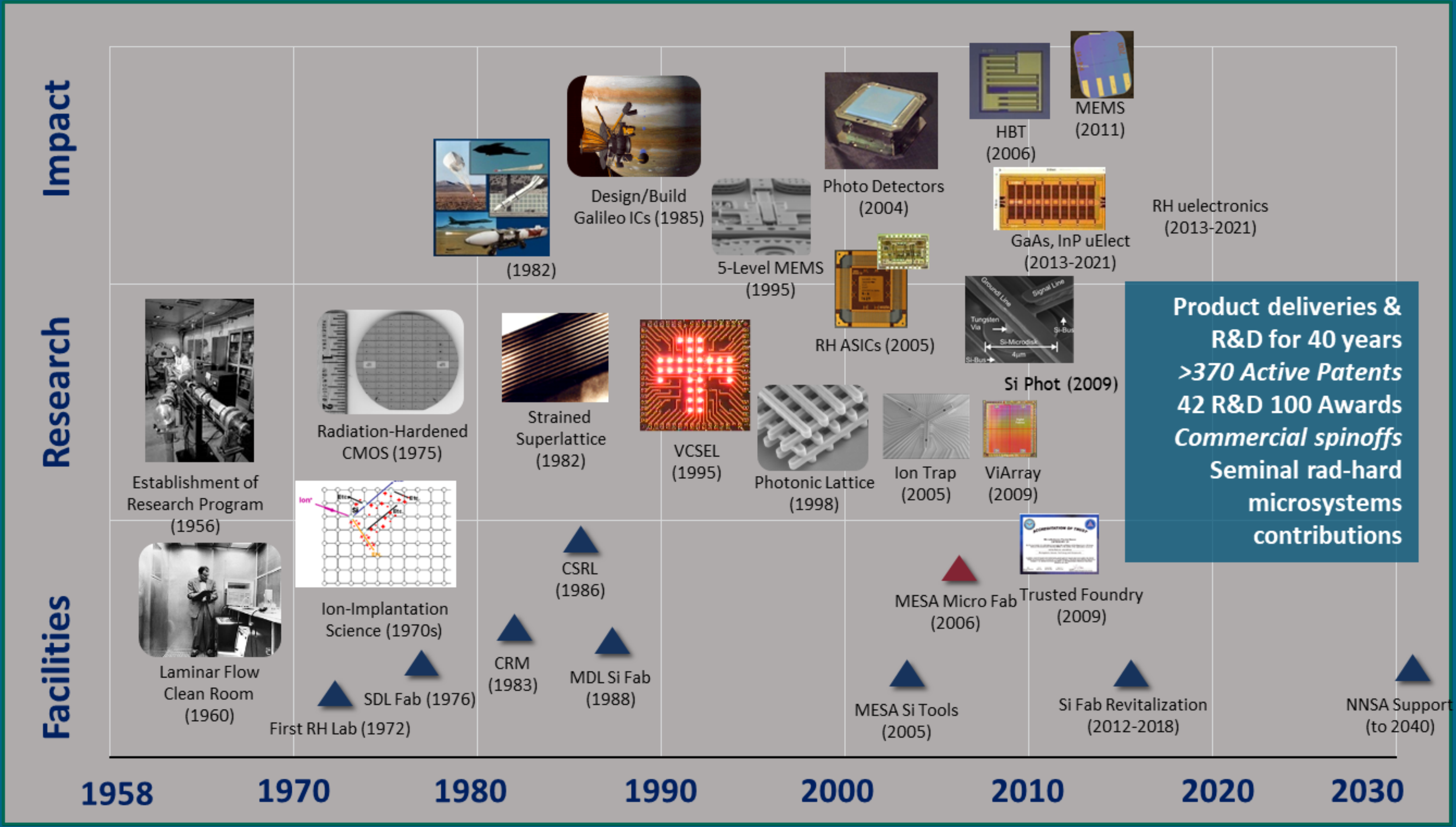
IBL

ION BEAM LABORATORY

RAD TEST FACILITIES

- ANNULAR CORE RESEARCH REACTOR (ACRR)
- SATURN ACCELERATOR
- HERMES III ACCELERATOR
- Z ACCELERATOR FACILITY

SNL's MESA Capability Arises from a Rich Legacy of High Impact Innovation



MESA Leadership is Enabled through Co-located Production and R&D

Hundreds of thousands parts across many products:

- Si CMOS ASICs
- III-V HBT SSICs
- MEMS Sensor
- Photonic Arrays
- Focal Plane Arrays
- RFICs (design & qualify)
- Optoelectronic device

Weapons & Satellites

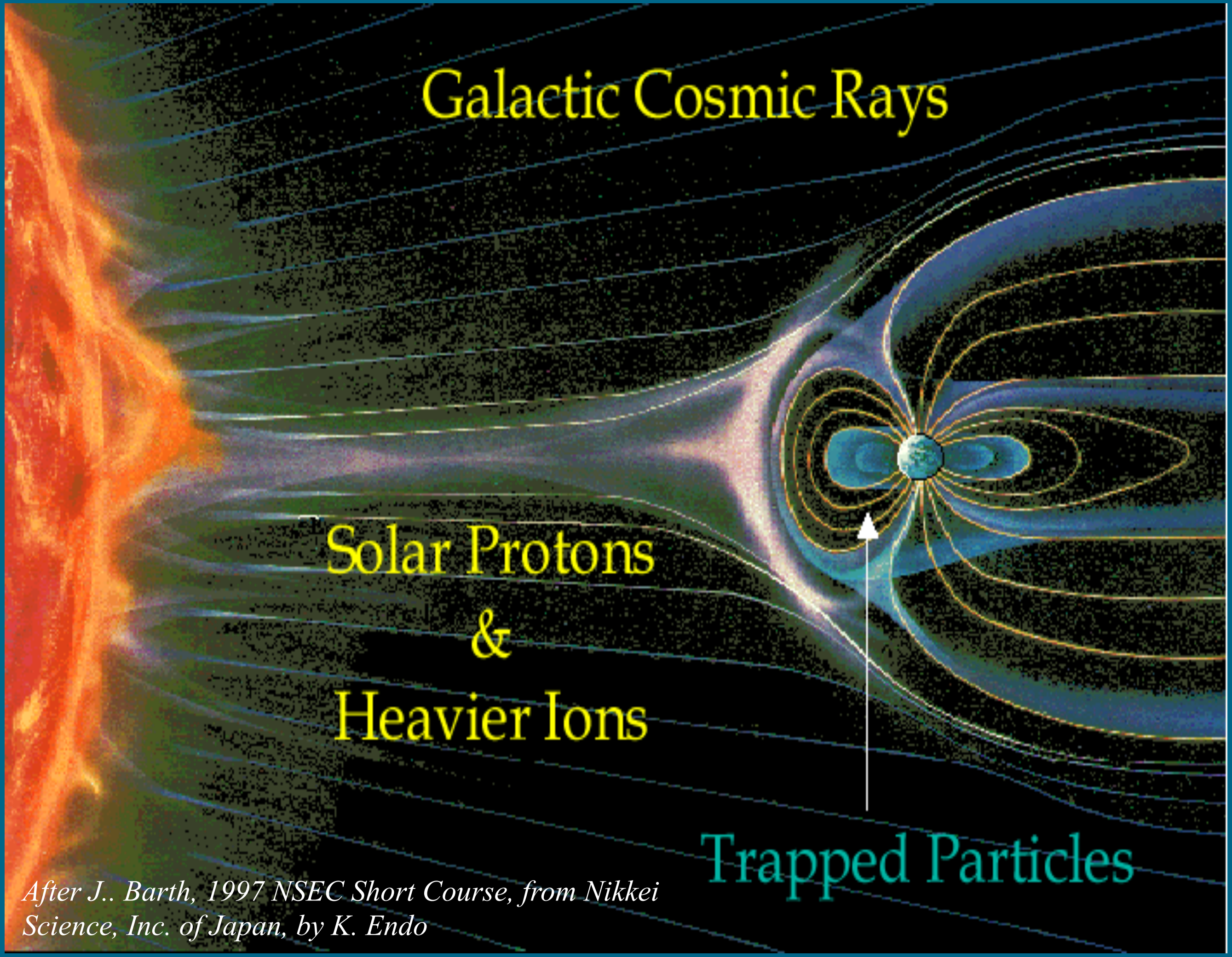
Research & Development | Si µElectr. | III-V µElectr. | MEMS | Photonics (Si, III-V) | Focal Plane Arrays | Heterogeneous Integration

Co-located R&D and Production

Research & Development
Design - Trusted Fabrication
Packaging - Radiation Effects Testing
Reliability/Qualification - Failure Analysis
Product Acceptance

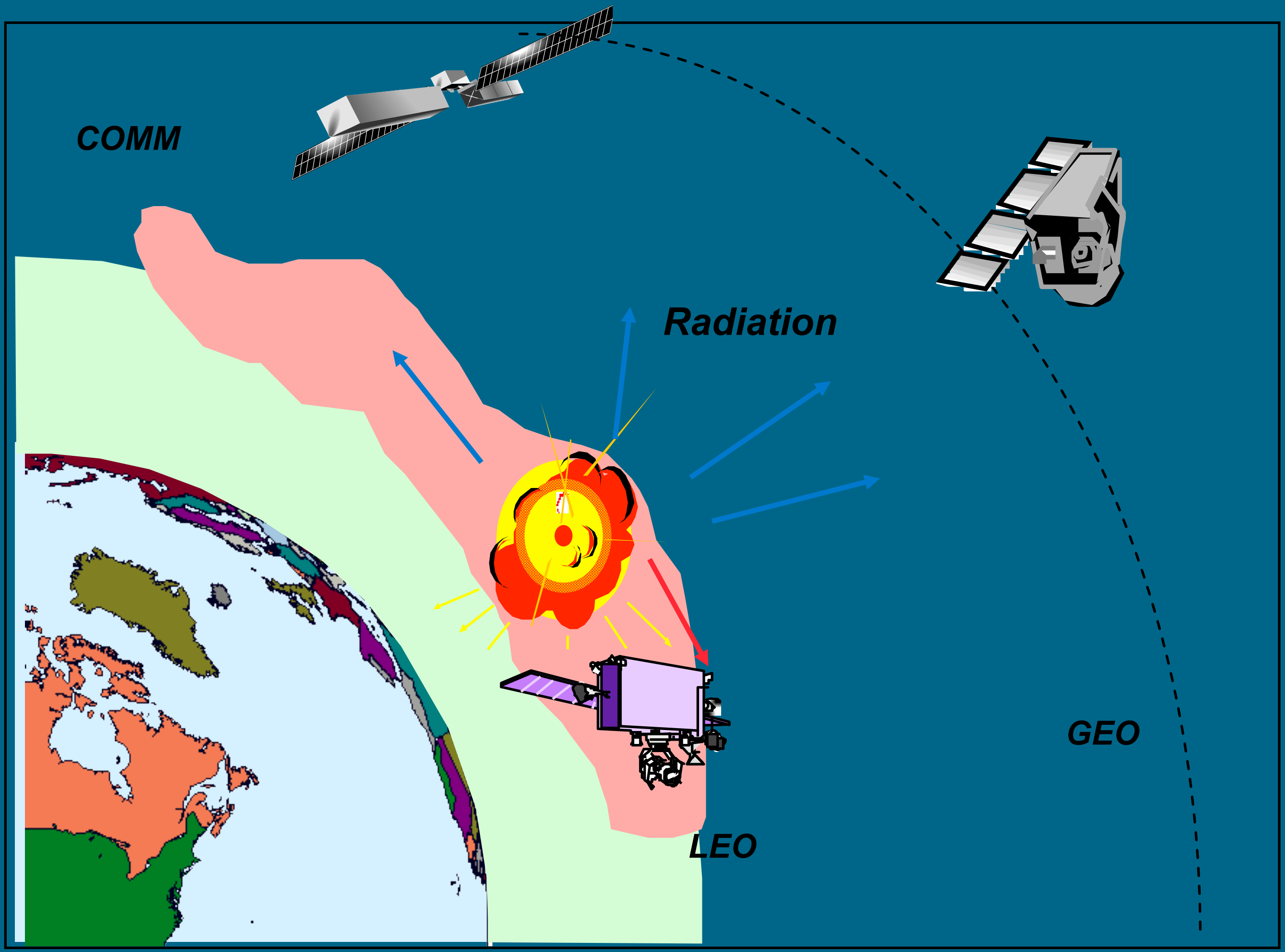
Microsystems Engineering, Science, and Applications (MESA)

National Security Assets Must Survive Natural Space Radiation Effects…

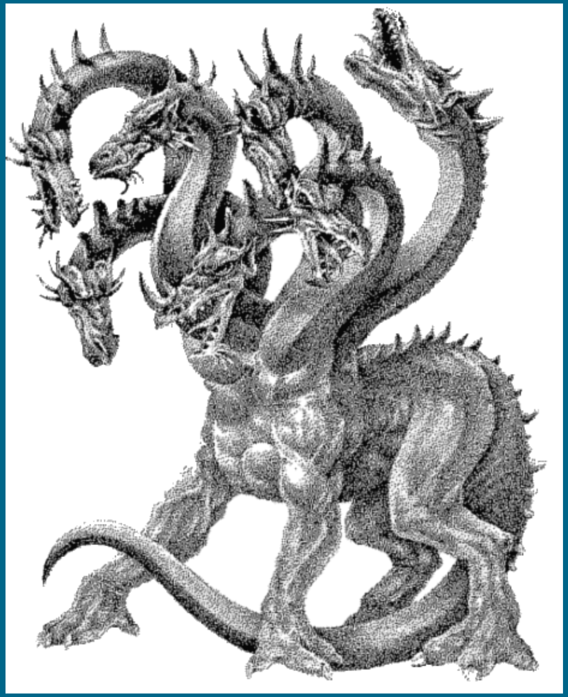


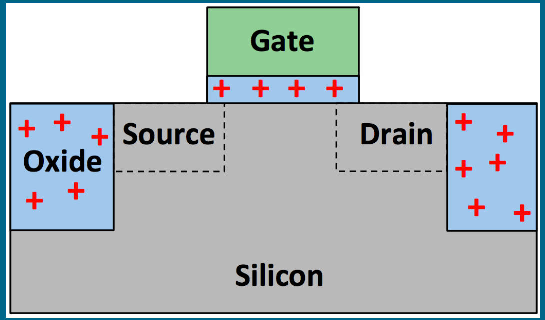
After J.. Barth, 1997 NSEC Short Course, from Nikkei Science, Inc. of Japan, by K. Endo

And Man-Made Radiation Environments

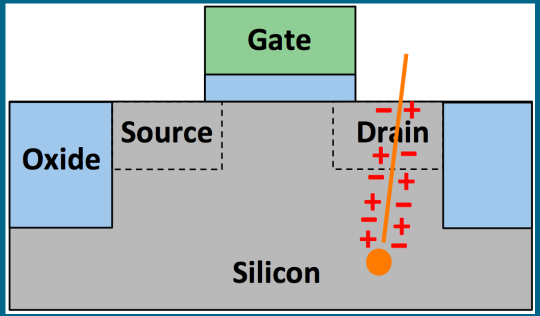


Radiation Causes Four Basic Effects in Microelectronics

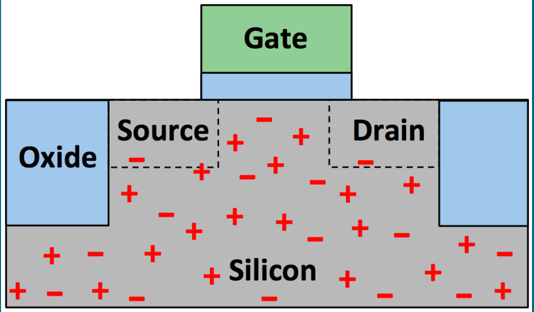




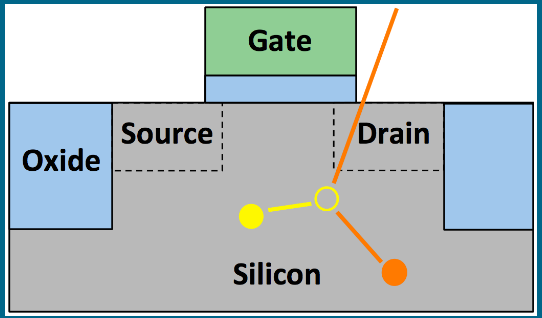
Total Dose Effects



Single Event Effects
Upset, Transient, Latchup



High Dose Rate Effects



Displacement Damage Effects

Innovative approaches are required to optimize tradeoffs between radiation hardness and system performance

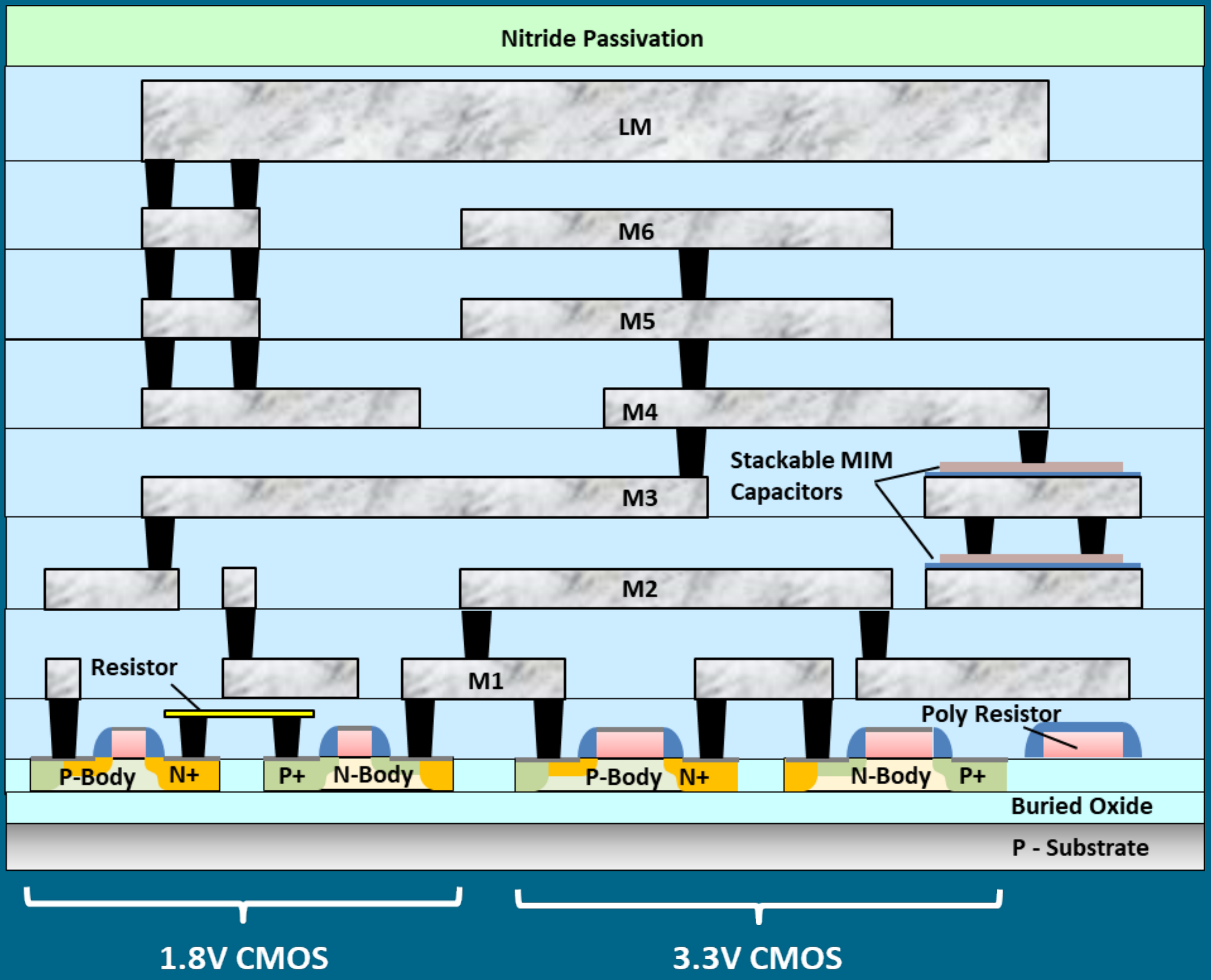
Opportunities to Explore and Integrate Hardness Assurance Abound Across the Spectrum of Semiconductor Manufacturing Nodes…

Increasing integration density

Tech	TID	SEL	SEU	SET	DD	DR
SNL A						
SNL B						
DOD A						
COM A						
DOD B						
COM B						
COM C						
COM D						
COM E						

LEGEND
Rad Hard
Needs Work
Unknown
Not Rad Hard

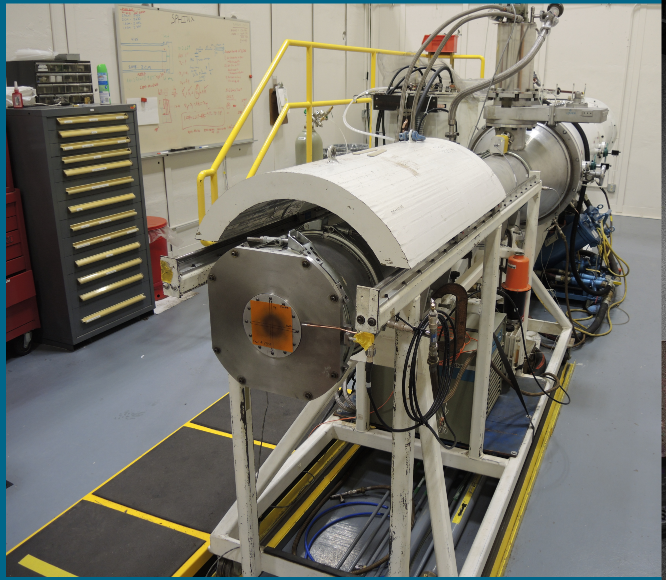
We Serve the Nation by Developing and Maintaining Trusted Radiation Hardened Process Technologies, for Example in Silicon CMOS…

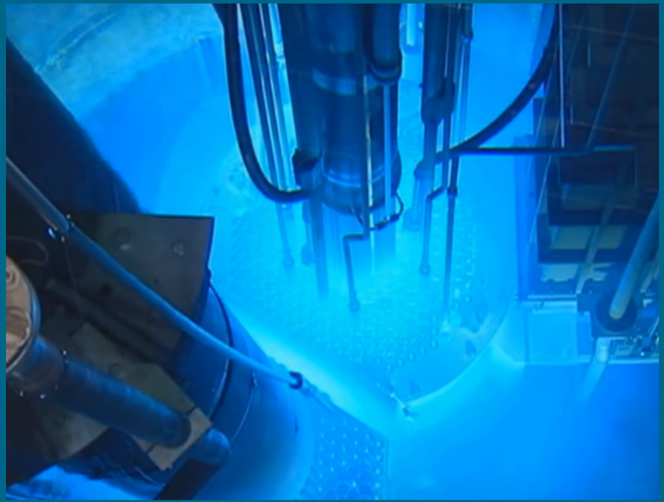


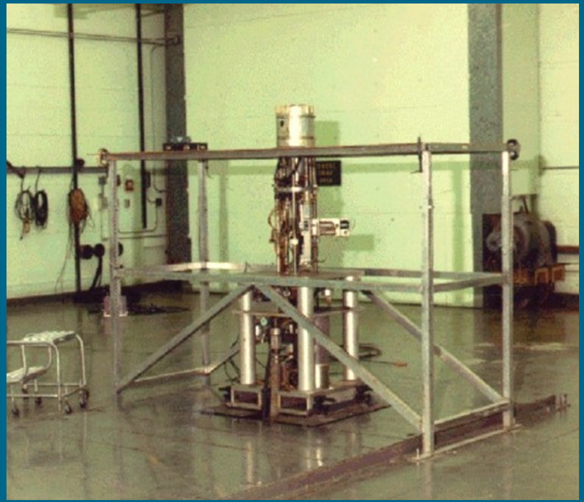
Our technologies have been successfully demonstrated in the harshest of environments

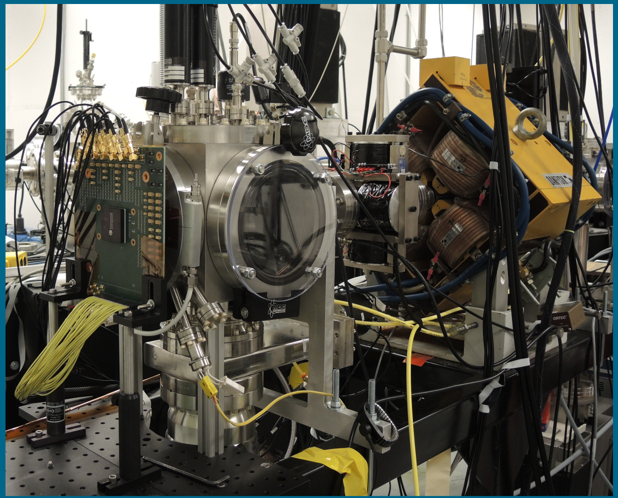
We Have 100's Years of Experience in Radiation Hardness Assurance at a Wide Variety of Radiation Environment Simulators, for Example…

- Little Mountain 958 Flash X-ray
- Sandia SPHINX facility
- Annular Core Research Reactor
- White Sands Fast Burst Reactor
- Sandia Ion Beam Laboratory
- TAMU Cyclotron
- And many others

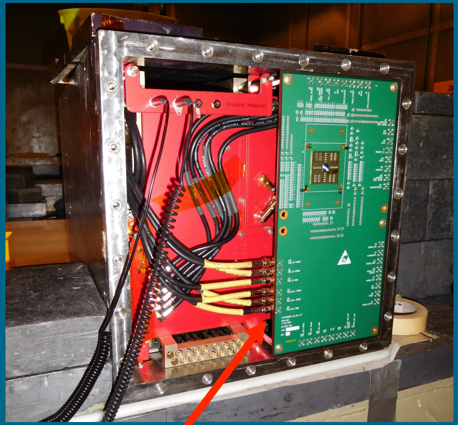


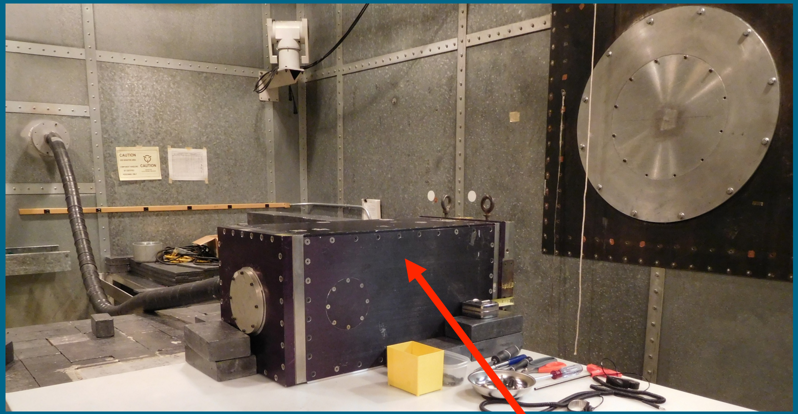






Testing in Harsh Radiation Environments is Challenging and Requires Precise and Careful Experimental Design and Execution

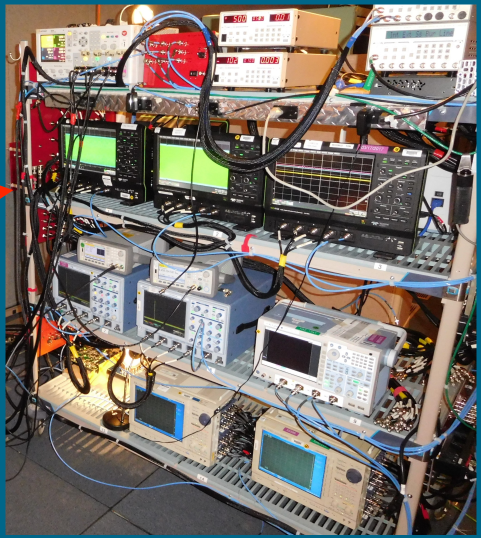




Test boards enclosed in a Sandia-designed Low-Noise RF Test Fixture

Test board and support electronics separated by ~50 feet of coaxial cables

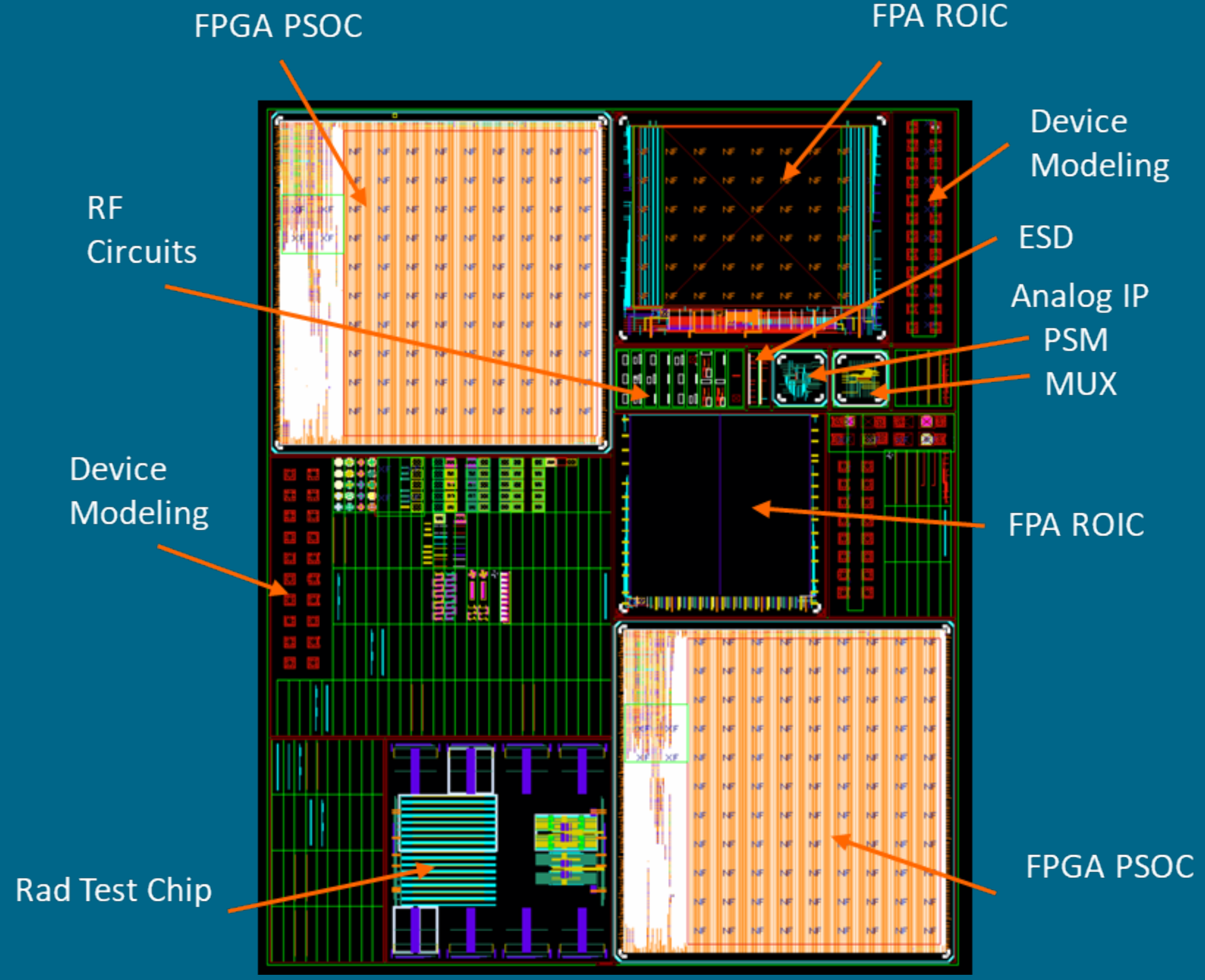
- 1 GHz operation possible because of on-chip clock generators and built-in self-test circuitry
- Support electronics included on FPGA evaluation boards and ARM ICE box



Diamond photoconducting detectors (PCDs) and high-speed oscilloscopes for pulse-shape measurements

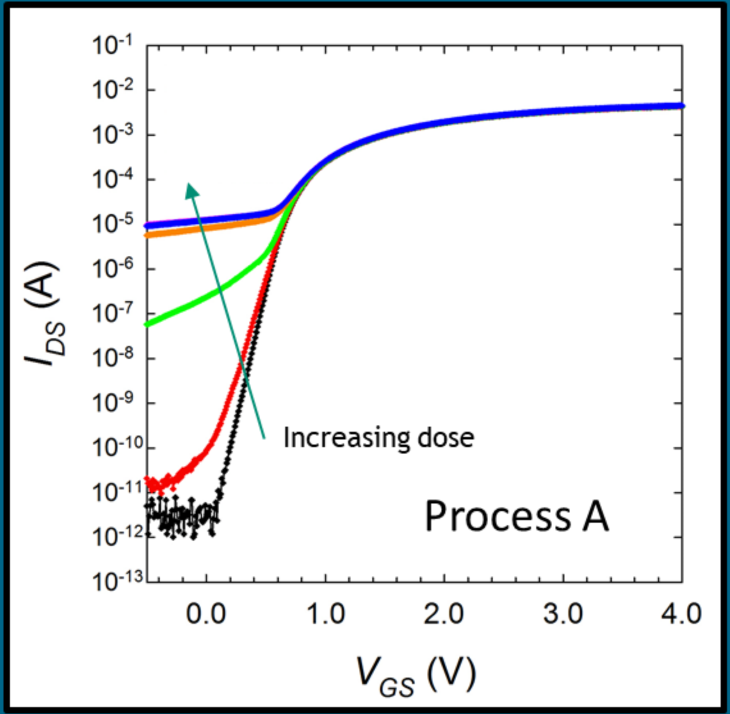
Thermoluminescent dosimeters (TLDs) to measure total dose

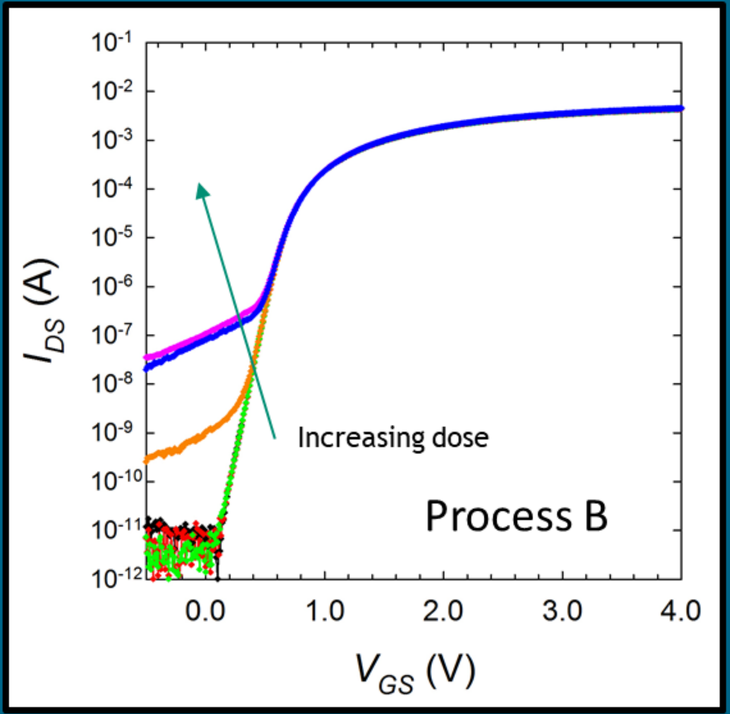
Innovative Integrated Circuit Design and Specialized Test Structures are Used to Demonstrate Mitigation Strategies and Hardness Assurance

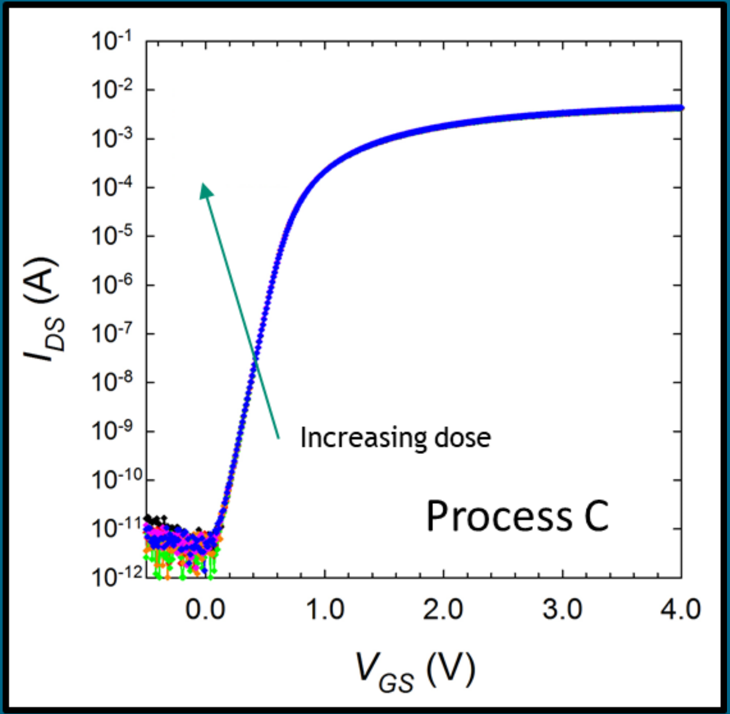


We run a Multi-Project Wafer (MPW) program for the benefit of many partners and customers

Intimate Access and Deep Technological Understanding Enable Robust Solutions for Radiation Hardened Applications



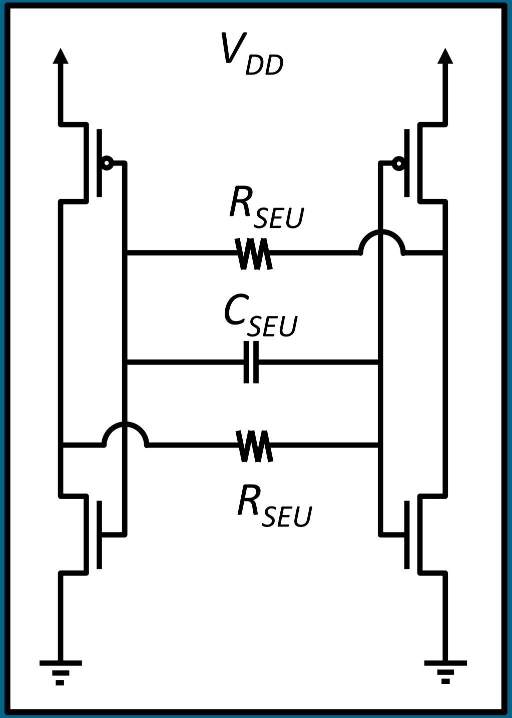




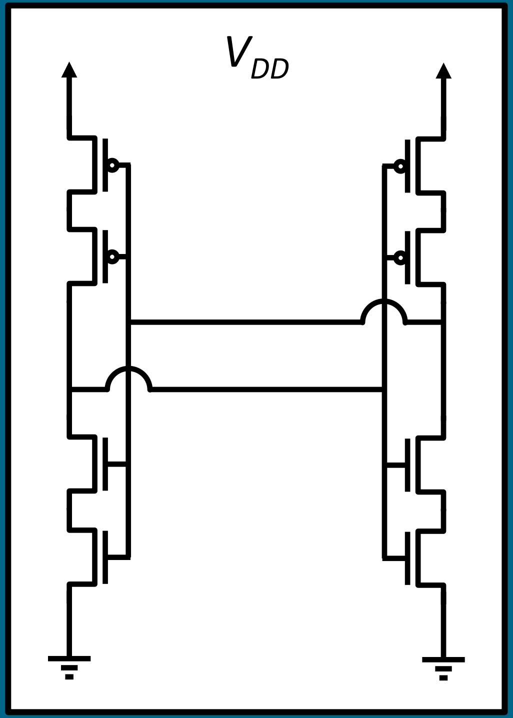
We routinely study process splits to improve transistor leakage from total ionizing radiation dose

Clever Circuit Architectures are Necessary to Prevent Single Event Upsets, Challenging Engineering to Maintain Product Performance

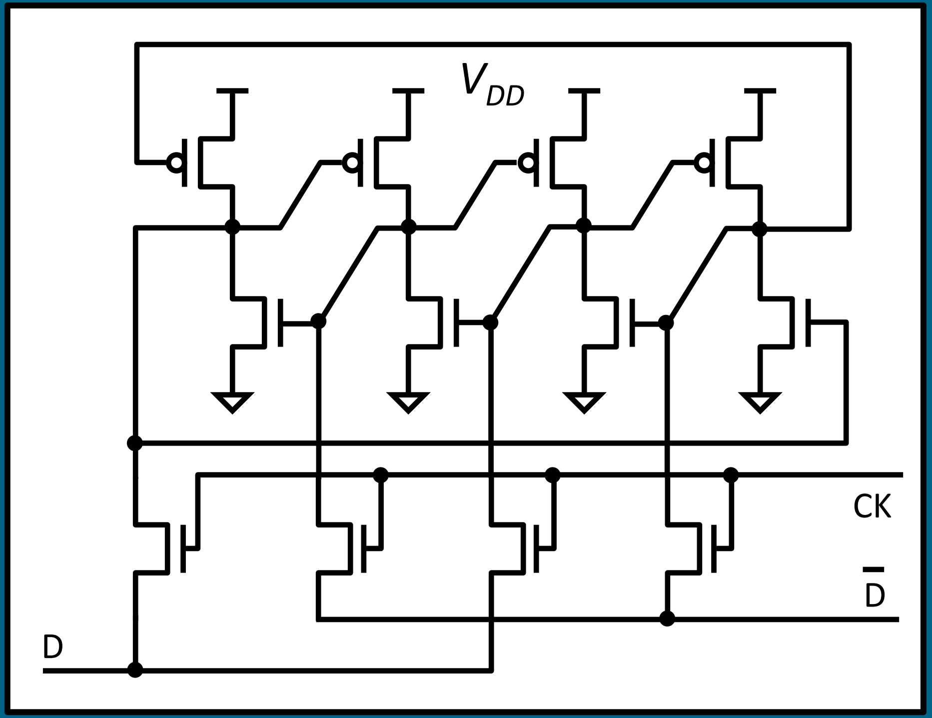
Single-event upset hardening approaches include RC delay hardening and design approaches based on either internal redundancy (e.g., DICE latch) or blocking current transients (stacked transistors)



RC Delay
(speed penalty)

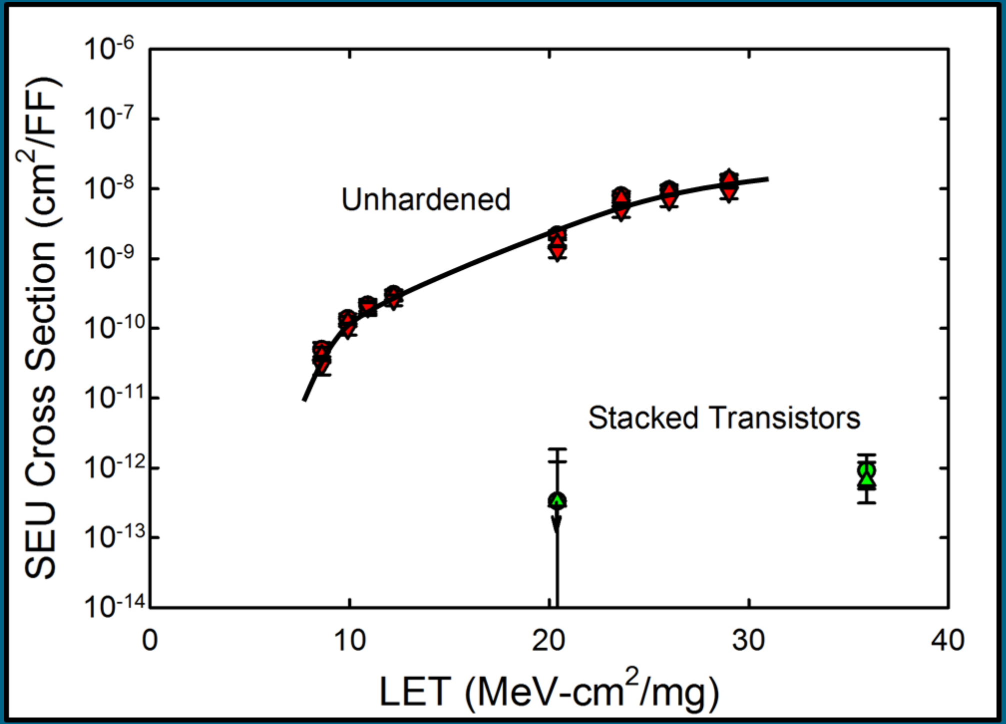


Stacked Transistors
(area penalty)



DICE Latch
(area penalty)

Heavy Ion Data Show that Stacked Transistor Approach Can Be Very Effective for Mitigating Single-Event Upset



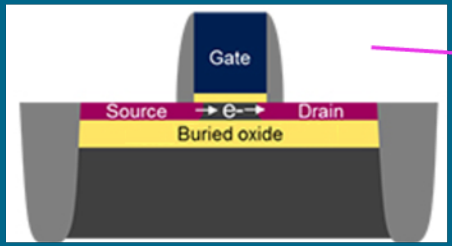
Texas A&M

15K DFF Chain
V_{DD} = 1.6 V
Static

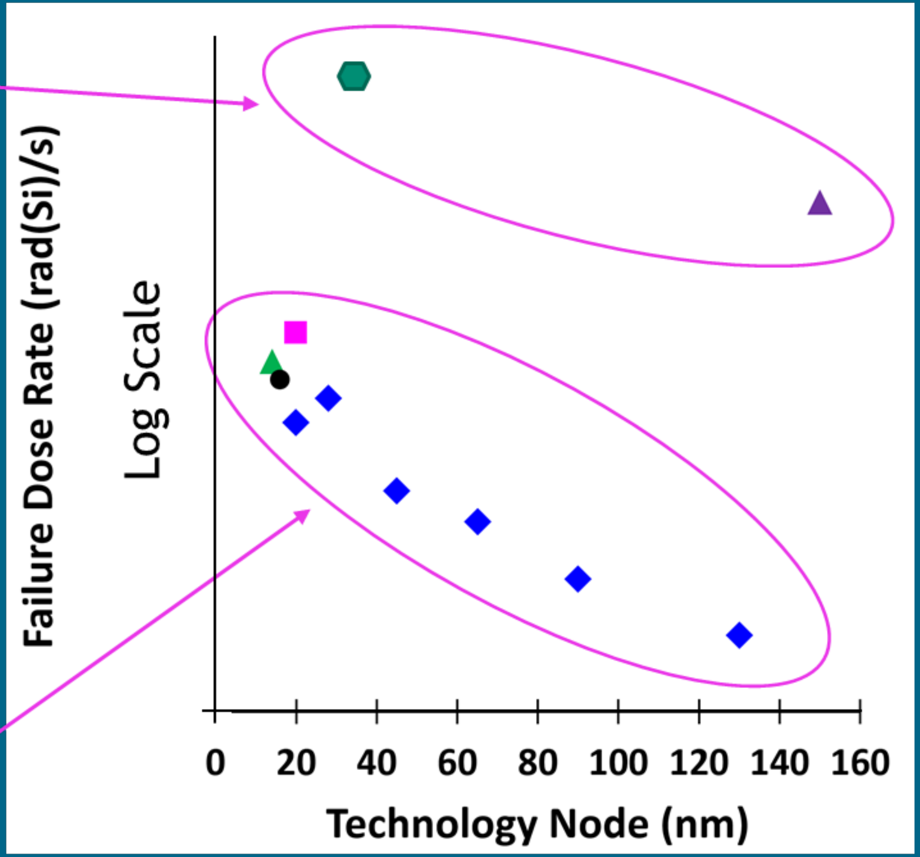
Due to large area penalty of stacked transistor approach, other optimizations are under investigation

At Sandia, We Have a Unique Mission in Radiation Hardening at the Extremes of the Possible, for Example Demonstrating Dose-Rate Performance in the Most Demanding Environments

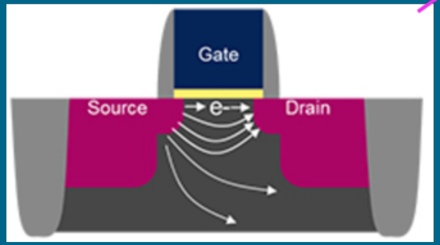
SOI substrate



- Scaling reduces sensitive volume dimensions



Bulk-Si substrate



We are leading the nation in discovering new mechanisms and new physics

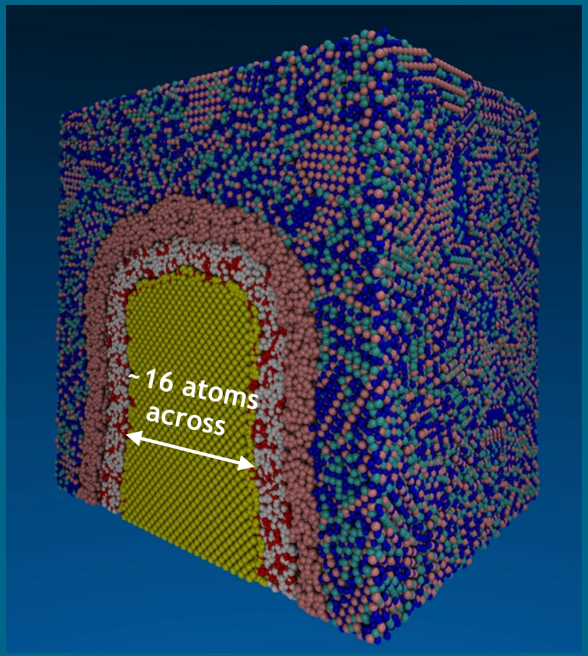
One Such Recent Discovery Shows CMOS Technology Has Scaled to the Point that it is Now Susceptible to Neutron Displacement Damage…

- Neutron displacement damage (nDD) introduces defects in the silicon lattice
  - Reduces minority carrier lifetimes → significantly affects minority carrier devices such as bipolar transistors
  - Metal-Oxide-Semiconductor (MOS) transistors are majority carrier devices
    - Usually not sensitive to nDD
    - Complementary MOS (CMOS) technologies are often not tested for nDD

- Highly Scaled CMOS may become susceptible to nDD
  1. Silicon feature sizes are now as small as DD clusters
  2. Silicon channels are very lightly doped (nearly intrinsic) in FinFET and Ultra-Thin-Body SOI technologies
     - Defects will cause larger effect in (new) lightly-doped transistors than in (old) heavily-doped transistors

- Design mitigations are an area of active research
  - Redundancy
  - Error Correction Techniques

Atomic level model of 14nm FinFET
[Aveyard & Rieger, EMC 2016]



Summary

- Sandia National Laboratories is a Leading R&D Institution with Compelling Mission Applications
- Our Nation Requires a Trusted, Assured, Reliable Supply of Microelectronics and Microsystems Components to Ensure its Security in Energy, Defense, Commerce…
- The Advanced Microsystems Radiation Effects Department is the Leader in Technology Development and Radiation Hardness Assurance for the Sandia MESA Capability
- NNSA has committed to the long term support of this capability and the Nation is increasingly turning its focus to ensuring strong on-shore microelectronics capabilities continue to exist
- Come help lead our nation in defining the future of microelectronics for national security